PHENIC: Silicon Photonic 3D-Network-on-Chip Architecture for High-performance Heterogeneous Many-core System-on-Chip

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***Abstract*—Network-on-chip architectures can improve the scalability, performance, and power efficiency of general multi-processor systems and application-specific heterogeneous multicore and many-core SoCs (MCSoCs). This interconnection paradigm when combined with 3D integration technology offers advantages over 2D NoC design, such as shorter wire length, higher packing density, and smaller footprint.**

However, since processor architects and semiconductor industries are heading towards complex and large system design consisting of hundreds of PEs, traditional fully 2D or 3D electronic NoC approaches are becoming not enough for providing significant large bandwidth with low-power consumption.

Optical Network-on-Chip (ONoC) promises significant advantages over their electronic counterparts. In particular, they offer a potentially disruptive technology solution with fundamentally low power dissipation that remains independent of capacity while providing ultra-high throughput and minimal access latency.

In this work, we propose a novel 3D hybrid architecture which uses optical layer for high bandwidth transfer and an electric control layer for path control. The architecture which is named PHENIC 3D-ONoC, is based on our earlier proposed 3D OASIS-NoC[1]. We present architecture, design, and preliminary evaluation results in a fair amount of details.

***Keywords*-optical interconnects; 3D-NoC; Many-core SoCs; Architecture, Heterogeneous Systems.**

I. Introduction

Embedded systems are moving towards the integration of hundreds of cores on a single chip and hold the promise of increasing performance through parallelism. As the number of cores integrated into an embedded chip increases, the on-chip communication becomes power and performance bottleneck in current and future embedded applications (cell phone, video, ...).

Network-on-Chip (NoC) architectures [1], [2], [3] have been proposed as a viable solution to meet the performance and design productivity requirements of these complex systems. In addition to simplifying the design of conventional systems, NoC has been also proposed to address other design/performance challenges, such as scalability, and wire delay problems.

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In recent years, many researchers [5], [28], [29], including our group [3], [4], investigated the architectures and design of two-dimensional electronic NoCs based on various types of topologies, flow-controls, and routing algorithms.

There have been also enormous efforts in 3D integration and 3D-NoCs designs to further address the interconnection delays problem and also the integration of disparate signals (analog, digital, or rf) or technologies (SoI, SiGe, HBTs, or GaAs) [27], [6]. By providing a third dimension of interconnect, wire delays can be substantially reduced. In addition, because for many high-performance applications, the performance bottleneck is often in the chip-to-chip or chip-to-memory communication, 3D integration offers the real advantage that massive amounts of bandwidth can be provided between device layers. This was helped by the recent advances in 3D integration technology in the area of heat dissipation cooling mechanisms, and through-silicon vias (TVSs), which cut across thinned silicon substrates to establish inter-die connectivity after die-bounding.

However, most proposed 2D/3D NoC architectures use copper based electrical interconnects as the physical level to transfer information between different components. Unfortunately, with DSM VLSI technologies, it is becoming increasingly difficult for copper based electrical interconnects to satisfy the design requirements of delay, power, and delay uncertainty [6], [31], [24], [5]. As a result, copper-based architecture may not scale beyond several tens of cores.

Future high-performance chips are expected to combine hundreds of components each integrated together to satisfy large and complex applications' power and performance requirements. Thus, to achieve significant and scalable solution to the interconnect delay problem, real fundamental changes in system interconnect, and fabrication technologies are needed.

Optical interconnect is an attractive solution for achieving ultra-high communication bandwidth in long-distance communication networks. However, this solution has not yet been widely investigated in chip-to-chip or in on-chip interconnections.
As the individual performance of main photonic devices

(i.e. photodetectors, modulators, waveguides, and lasers) significantly improves recently, there is a growing interest in addressing the issues of photonic and CMOS devices integration [13], [14], and new applications for a converged electronic-photonics IC platforms are being developed [15], [16], [17], [18], [19].

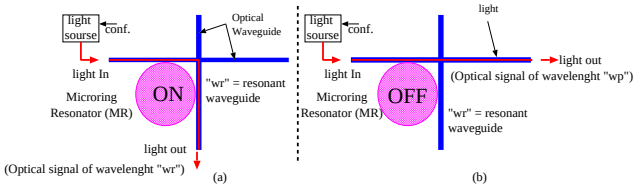

Figure 1. Optical Switch.

Optical Network-on-Chip (ONoC) is a novel concept enabling high bandwidth especially when combined with Wavelength Division Multiplexing (WDM) to concurrently transfer multiple parallel optical stream of data through a single waveguide, which contrast with ENoC that requires a unique metal wire per bot stream.
In ONoC, optical switch and waveguides are used to realize the same function as a conventional electrical router but with routing based on wavelengths. The routing and flow control are managed in electronics.

Furthermore, ONoC offers a potentially disruptive technology solution with fundamentally low power dissipation that remains independent of capacity while providing more bandwidth at near speed-of-light transmission latency. The key power saving comes from the fact that once a photonic path is established, the optical data are transmitted end to end without the need for buffering, repeating, or regenerating [34], [33], [37], [39], [24], [25], [26]. This is different from electronic NoCs, where message are buffered, regenerated and then transmitted on the inter-router links several times en route to their destination [37]. In addition photonic routers do not need to switch with every bit of the transmitted data like in electronic routers; optical routers switch on and off once per message, and their energy dissipation does not depend on the bit rate. This feature allows the transmission of ultra high bandwidth messages while avoiding the power cost which found in traditional electronic networks [37].

In this work, we propose architecture and preliminary evaluation results of a new 3D photonic NoC (PHENIC 3D-ONoC) for application specific many-core SoCs (MCSoC). PHENIC architecture is based on our earlier proposed electronic 3D-OASIS Network-on-Chip (OASIS 3D-NoC) [10], [9], [7], [8].

II. Related Work

Due to technology limitation, photonic NoC architecture is bufferless in the foreseeable future. The circuit-switched nature of photonic interconnect directly affects the performance and power characteristics of on-chip communication. Briere et al. [34] proposed a multistage ONoC with a passive switching $\lambda router$. Kirman et al. [33] presented a hierarchical optical bus for multiprocessor systems. The optical loop encircles the chip with wavelength division multiplexing support at the top level of the hierarchy. Shacham et al. [37] presented an optical NoC architecture based on augmented-mesh and a blocking 4×4 optical switch. The network is circuit-switched and some critical network design issues such as path-setup and tear-down are covered in the work. Beausoleil et al. [36] proposed a crossbar based ONoC, where 64 wavelengths are multiplexed over 270 waveguides. Work in [11] proposed to use an optical ring waveguide with bus protocol standards to replace global pipelined electrical interconnects. Mo et al. [38] proposed a hierarchical mesh-based ONoC. The architecture uses hybrid optical-electronic routers for electronic wormhole switching in local networks and circuit switching in the global mesh-based optical network.
Pan et al. [52] presented a high throughput optical crossbar-based on-chip network architecture with localized arbitrations. Cianchetti et al. [39] presented an optical network with a predecoded source routing mechanism. Low latency is achieved by transmitting packets several hops in a single clock cycle if no contention exists. Gu et al. [45] proposed a fat-tree based ONoC.
In [40], Kodi et al. proposed an ONoC architecture for 64 cores. The bandwidth is maximized with the proposed static routing and wavelength allocation schemes. In [41], Ding presented an optical routing framework to reduce the power consumption of ONoCs. Batten et al. [42] proposed an optical mesh based on a hybrid optical-electrical global crossbar, where the processing cores and DRAM are divided into sub-meshes and connected with the optical crossbar. In [43], silicon MRs of small size have been demonstrated. The fabrication is based on silicon waveguides with a cross-section of 500-200 nm and the insertion loss is about 0.5 dB.
Experiment results show that the MR on/ff switching power consumption is on the order of $20\mu W$ [44]. Ji et al. [46] presented a non-blocking 5×5 optical router. The router uses 16 MRs in total. One MR should be turned on for every switching, except for switchings from east to south, or south to east, or west to north, or north to west.

There are also several works about electronic 3D-NoCs. Our group proposed and designed in [9], a so called OASIS 3D-NoC based on mesh topology and look-ahead fault tolerant (LAFT) routing algorithm. Feero et al. [47] evaluated the performance of 3-D electronic NoCs with 3-D mesh and fat-tree topologies. It was found that the 3-D realization of both mesh and fat-tree based NoCs could improve the performance significantly with higher integration densities

and smaller footprints. In [50], Chen et al. proposed a 3D-NoC architecture based on De-Bruijn-Graph to achieve smaller network diameter and smaller network latency.

In addition to researches about electronic 3D-NoCs, there are also several research works on the 3D-ONoC architectures. Gu et al. [45] proposed a 3-D optical cubic-mesh NoC together with an optimized partial crossbar based optical router. In [24], [25], [26], authors proposed the design of passive routing 6×6 and 7×7 optical routers and propose optimized floor-plans for the 3-D mesh-based ONoCs.

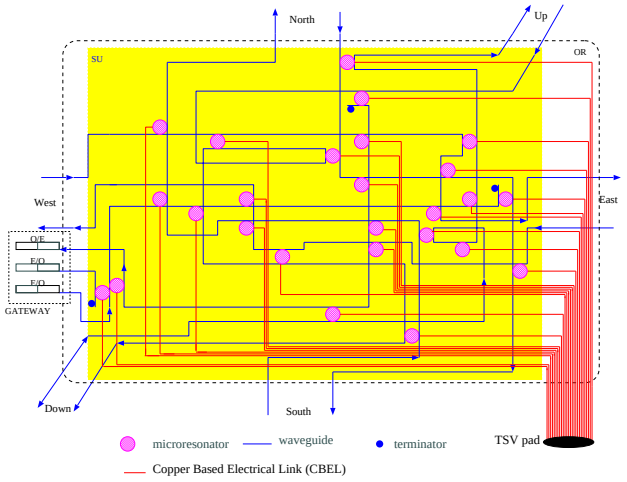

Figure 2. PHENIC's Optical Router Organizaation.

III. PHENIC Optical Router Architectures

The most prevalent photonic network element of PHENIC architecture is the non-blocking seven-port bidirectional router, which dynamically routes broadband messages to their destinations. Microresonator (MR) is used as a simple component to implement the basic 1×2 switching element. A given MR element has a resonance wavelength λmr, which is determined by the material and structure of the microresonator. When the wavelength λmr of a given optical signal is equal to the resonance wavelength λmr_{res} of the microresonator, the optical signal will make turn as shown in Fig. 1 (left). Otherwise, it will pass by the microresonator and will continue on the same direction (Fig. 1 (right).

PHENIC's optical router block diagram is shown in Fig. 2. It is based on multiple optical switching elements and consists of a switching unit (SU) and control unit (CU) modules. The SU is a simplified module of the typical 7×7 crossbar. One important feature of PHENIC router is that in addition to the basic 1×2 based switching elements with crossing waveguides, it also used those with parallel waveguide structure to reduce the waveguide crossing insertion loss. In addition careful design have been made to reduce waveguide crossings inside the switching fabric inside the SU.

The control unit is made up of a centralized control unit (CU) and 7 (one for each direction: EAST, WEST, NORTH, SOUTH, UP, DOWN) control (EOC/OEC) interfaces (Gateways). The CU uses electrical signals to configure the switching fabric via an electronic network according to the routing requirement of each packet (discussed later).

IV. System Architecture

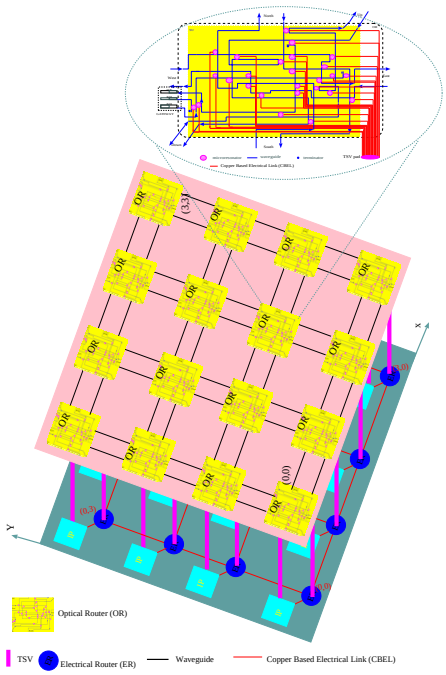

Figure 3. PHENIC Architecture.

PHENIC architecture is based on 3D-Mesh topology for interconnecting several tiles. The architecture realizes the same functions as classical electrical NoC (i.e. our earlier developed 3D-OASIS-NoC [10], [9], [7], [8]) but with routing based on wavelength. That is, within each optical router, the route followed by a packet depends on the wavelength of its carrier signal (and not on information either contained in the packet or traveling along with it).

The simplified block diagram of the system architecture is shown in Fig.3. The system consists of two type of networks. The upper one is the Photonic Communication Network (PCN) and is based on silicon broadband photonic switches interconnected by waveguides. Each optical interconnect is 1 bit wide and bidirectional. The PCN routes packets of optical signals accross the chip,

with low latency and low power dissipation (described later).

The bottom layer is called Electronic Control Network (ECN) and is used for path reservation and configuration of the optical routers at the PCN layer. The ECN is also responsible for exchanging short electrical messages among processor cores. It uses bidirectional 32-bit wide electrical lines for configuration by mainly powering ON/OFF the MRs.

As indicated in Fig.3, each IP core is connected to a local electrical router and also connected to the corresponding gateway (modulator/detector) in PCN via special TSV. Messages generated by the IP cores are separated into control signals and payload signals. Control signals are routed in the ECN network and used for path setting (routing). While the payload ones are converted to optical data and transmitted on the PCN network. As we earlier mentioned, each electrical router sends control signals to the appropriate optical router through dedicated TSV to power ON/OFF the MRs and to adjust the wavelength conversion. The ECL network is based on conventional CMOS transistors and was built in hardware. Fig. 4 shows the floor-plan of the ECN network.

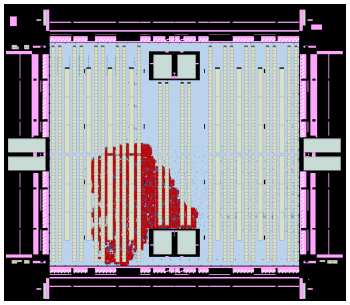

Figure 4. Floorplan layout of PHENIC's $6 \times 6 \times 2$ ECN. The ECN is designed to work at high clock frequency with 32-bit wide bidirectional interconnects.

A. Gateway

In PHENIC system, each IP core is connected to a *gateway* which enables the electro-optical conversion. Fig. 5 illustrates the block diagram of the *gateway* circuit. As shown in the figure, it consists of two modules: (1) Transmitter Module (TM), and (2) Receiver Module (RM). The TM is composed of a serializer (SER), drivers, lasers, and multiplexer (not shown for simplicity). While the RM is composed of demultiplex, PIN photo-diodes, trans-impedance amplifier (TIA), and deserializer (DESER).

B. Optical Path Setting

Before sending the optical data packets, the source node (transmitter) first issues a configuration (path setting) packet via a *Copper-Based-Electrical-Link* (CBEL) to the destination node (receiver). The configuration packet is routed via the ECN network, reserving the photonic switches along the path for the photonic message (payload) which will follow it. It includes a destination address information, and other additional control information. The routing is based on our LAFT (Look Ahead Fault Tolerant) routing algorithm [9]. LAFT performs the routing decision for the next node taking into consideration its electrical link status and selects the best minimal path. In order to deliver any control flit from source to destination nodes, LAFT assumes that the links connecting the components to the local input and output ports are always non-faulty, and there exists at least one minimal path between a $[Src, Des]$ pair (discussed later in more details). When the destination node receives the

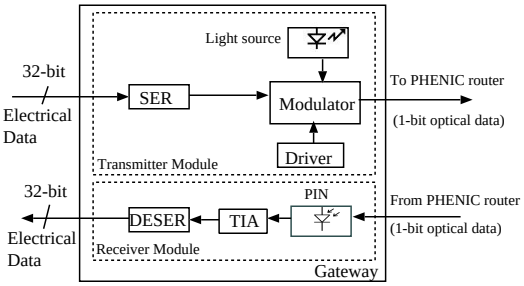

Figure 5. Gateway Organization.

configuration packet, it will acknowledge that the optical path setup is done. In order to fully utilize the capability of the implemented bidirectional optical waveguides, the receiver sends a small light pulse back to the sender on the optical waveguide. When the small ACK light pulse is received and processed, the source node, then, starts transmission of optical data packets via the waveguides. Finally, when the transmission is finished, the reserved path would be released (tore down) **by a release packet**.

By using such circuit switching communication protocol, no buffer is needed for the optical data and also the latency performance is guaranteed. As with other photonic NoCs, PHENIC performs better with larger message sizes due to the high speed of transfer (speed of light) in the optical network once the communication path is established. Furthermore, data in PHENIC arrives at the destinations in the same order as they are generated and, so, there is no need to reorder packets at the destination nodes.

C. PHENIC Photonic Building Blocks

Lasers, modulators, photodiodes, and waveguides are all passive elements and are the main building blocks of PHENIC's gateway and PCN network. Bellow, we describe these components in details.

1) Lazer Source: Since there is no available high-speed, electrically driven, on chip monolithic laser light [5], [12], PHENIC features an off-chip laser source, such as VCSEL (Vertically Cavity Surface Emitting Laser).

As indicated in Fig. 1 (a), the off-chip laser source provides light to the modulator(s), which transducers electrical information into a modulated optical signals. Then, when the lights enter the chip, optical splitters and waveguides route it to the different modulators used for data transmission.

2) Modulators: Before messages are transmitted on the PCN network, the electrical messages from each IP core should be converted to optical form. PHENIC implements at each node a *Gateway* (Fig. 5) serving as a photonic network interface and based on silicon optical modulators [48], [12] and SiGe photodetectors [49], [12].
To reduce conversions time, modulators should be small (i.e. the circular shaped $10\mu m$ ring-modulator [22]) and fast. The performance of a typical modulator is dependent on the on-to-off light intensity ratio [5], which depends of the electrical input signal strength. A higher extinction ratio is better and required for fast and accurate signal detection. Works in [22], [5] reported that an extinction ratio greater than 10dB is acceptable and enough to enable proper signal detection without causing communication errors.

3) Waveguide: The waveguides provide the physical interconnection between all sources and destinations and enables connectivity between all photonic devices in PHENIN systems. The transmitter demultiplexes the light into appropriate wavelength channels and then modulates each of the channel with a digital data stream generated by the electronic component to be interconnected. Finally, photonic signals are routed to various PEs via routers and waveguides.
We have to note here that the *refractive index* [5] of the waveguide material has a big impact of the bandwidth, latency, and area of an optical interconnect. A waveguide typically has a width of $0.3\mu m$ [35].
Once the photonic signals are received by the destination node (receiver), the signals must be converted back to electrical form by the *gateway*. In addition, since PHENIC simultaneously transmits different wavelengths per bidirectional waveguides, a wave selective filter for each received wavelength is needed at the destination node.

4) Microring Resonator Active Elements: The main element of PHENIC and other silicon photonic systems is the microring resonators (MRs) (Fig. 1). MRs are capable of effectively guiding the path an optical signal will take through careful design of the dimensions and position of the resonator. Optical signals couple into ring resonators at specific regularly spaced wavelengths in the optical spectrum, called resonant modes [54]. The MRs are the backbone components of the optical router in PHENIC system.

Algorithm 1: LAFT Routing Algorithm for PHENIC's Optical Path Setting

```
// Destination address
Input: X_dest, Y_dest, Z_dest
// Current node address
Input: X_cur, Y_cur, Z_cur
// Next-port identifier
Input: Next-port
// Link status information
Input: Fault-in
// New-next-port for next node
Output: New-next-port
// Calculate the next-node address
Next← Next-node (X_cur, Y_cur, Z_cur, Next-port);
// Read fault information for the next-node
Next-fault← Next-status (Fault-in, Next-port);
// Calculate the three possible directions for the next-node
Next-dir← poss-dir (X_dest, Y_dest, Z_dest, Next_x, Next_y, Next_z);
// Evaluate the diversity number of three minimal paths
Div_1 ← path-div (X_dest, Y_dest, Z_dest, poss − dir_1);
Div_2 ← path-div (X_dest, Y_dest, Z_dest, poss − dir_2);
Div_3 ← path-div (X_dest, Y_dest, Z_dest, poss − dir_3);
// Evaluate the New-next-port direction
if (|Next-dir| > 1) then
    if (Div_1==Div_2==Div_3) then
        New-next-port ← min-congestion (poss − dir_1, poss − dir_2,
        poss − dir_3);
    else
        New-next-port ← max-diversity (poss − dir_1, poss − dir_2,
        poss − dir_3);
    end
else
    if (Next-dir == 1) then
        New-next-port← Next − dir_1;
    else New-next-port← nonminimal (X_dest, Y_dest, Z_dest, X_cur, Y_cur, Z_cur,
    Fault-in);;
end
```

D. Routing Algorithm

As we mentioned in the previous section, the communication path should be acquired first before sending the photonic signals (payload) on the PCN. This operation requires a configuration packet to travel a number of electronic routers and undergo some routing decision in each hop. Additionally, the configuration packet may experience blocking (i.e., due to some faults) at certain points in its path further contributing to the setup latency.
Once the path is acquired, the transmission latency of the optical data is very short and depends only on the group velocity of light in a silicon waveguide (approximately $6.6 \times 10^7 m/s$ for a 2-cm path crossing a chip [51]).

The path-setup procedure is based on our earlier proposed LAFT routing algorithm [9], [7], [8], which performs the routing decision for the next node taking into consideration its channel status and selects the best minimal path. The above routing scheme is illustrated in Algorithm 1. In the first phase, LAFT calculates the next node address depending on the next-port identifier read from the flit. For a given node wishing to send a configuration flit to a given destination, there exist at most 3 possible directions through X, Y, and Z dimensions, respectively. In the second phase, LAFT performs the calculation of these 3 directions by comparing x, y and z coordinates of both current node and

destination node concurrently. At the same time, as these directions are being computed, the fault-control module reads the next-port identifier from the flit and sends the appropriate fault information to the corresponding input-port. By the end of this second phase, LAFT has information about the next node fault status and also the three possible directions for a minimal routing. In the next phase, the path-setup routing selection is performed. For this decision, we adopted the following prioritized conditions to ensure fault-tolerance and high performance either in the presence or absence of faults:

1) The selected direction should ensure a minimal path, and it is given the highest priority in the routing selection.
2) We should select the direction with the largest next hope path diversity.
3) The congestion status is given the lowest priority.

Depending on these priorities, LAFT reads the fault status of the next node received from the fault-control module and checks the number of possible non-faulty minimal directions. As illustrated in Algorithm 1, if only one non-faulty minimal direction is obtained, this direction will be selected as out-port for the next node. If more than one possible minimal direction is available, the algorithm selects the direction which leads to a node with higher path diversity. The diversity value for a given node is the number of possible directions leading to the destination through a minimal path [32]. A node with high diversity results in more routing choices. This means that the probability of finding a non-faulty link is greater when considering faults. When no faults are detected in the system, selecting the direction with the highest diversity gives more choices to find the least congested direction.

As stated in [32], to obtain directions with high diversity, we should select those leading to nodes located in the center of the mesh and avoid routing to the edges of the network When the three possible directions are minimal and have the same diversity, the routing selection is made depending on the congestion of each output port. This congestion information is obtained by the *stop* signal issued from the flow control used in our system. When there is no valid minimal route available, LAFT chooses a non-minimal route while also considering the 2nd and 3rd priorities (path diversity and congestion) as illustrated in algorithm 1.

Table I
PHENIC's ECN Hardware Complexity

Architecture	Optimization Type	Target Device	Area (ALTU/HCells)	Power (mW)
ECN	Area	FPGA	61,383	1351,25
		STRUCT-ASIC	408,040	451,78
	Speed	FPGA	73,222	1464,70
		STRUCT-ASIC	473,958	465,76
	Balanced	FPGA	72,154	1406,65
		STRUCT-ASIC	504,782	473,61

V. Conclusion and Future Work

Optical Network-on-Chip (ONoC) promises significant advantages over their electronic counterparts. In particular, they offer a potentially disruptive technology solution with fundamentally low power dissipation that remains independent of capacity while providing ultra-high throughput and minimal access latency.

This technical report presented architecture and preliminary hardware design and evaluation of a novel 3D Optical Network-on-Chip architecture, named PHENIC. Future work will focus on evaluation of the whole PHENIC system using real benchmark programs. To understand the real merits of PHNEIC system, complete evaluation of the througput and power are under investigation.

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Heterogeneous manycore architectures are the key to efficiently execute compute- and data-intensive applications. Through silicon via (TSV)-based 3D manycore system is a promising solution in this direction as it enables integration of disparate computing cores on a single system. Recent industry trends show the viability of 3D integration in real products (e.g., Intel Lakefield SoC Architecture, the AMD Radeon R9 Fury X graphics card, and Xilinx Virtex-7 2000T/H580T etc.). However, the achievable performance of conventional through-silicon-via (TSV)-based 3D systems is ultimately bottlenecked... The performance of the modulators is also dependant on the access resistance, in series with the reverse-bias pin diode capacitor. The challenge is to get low optical losses and low RC constants in Mach-Zendher or Fabry-Perot interferometer configurations. The variation of the effective index due to carrier depletion has been measured at.Â This technique is often called 3D heterogeneous integration because the CMOS part is separated from the photonic part without any silicon surface waste at the transistor level. With this approach, any microelectronics technologies can be used for the electrical parts and IIIâ€“V components can be embedded in the photonic layer.Â Even with the latest development on active silicon photonics, IIIâ€“V components remain more efficient for light-matter interaction. PHENIC: Silicon Photonic 3D-Network-on-Chip Architecture for High-performance Heterogeneous Many-core System-on-Chip. September 2013. DOI:10.13140/RG.2.1.1075.0563.Â Network-on-chip architectures can improve the scalability, performance, and power efficiency of general multi-processor systems and application-specific heterogeneous mul-ticore and many-core SoCs (MCSoCs). This interconnection paradigm when combined with 3D integration technology offers advantages over 2D NoC design, such as shorter wire length, higher packing density, and smaller footprint.